REMARKS

A Schedule of Amendments is submitted herewith.

Should the examiner find any parent claim to non-elected claim 20 to be allowable, the Examiner is respectfully requested to examine claim 20.

The specification title and abstract are amended in response to the Examiner's objections thereto.

Claim Objections

Claims 13-18 are amended in response to the Examiner's objections.

Claim Rejections - 35 USC 112

Claims 15-18 are amended in response to rejections under 35 USC 112.

Claim Rejections - 35 USC 102

Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by US patent 5,832,600 (HASHIMOTO). Claim 13 (as amended) is patentable over HASHIMOTO for the reasons indicated below.

The invention as recited in claim 13 is a method for fabricating an interconnect system providing a signal path to a node on an IC fabricated within and on an upper surface of a semiconductor wafer, wherein the signal path extends to the lower surface of the wafer material. Claim 13 recites forming a hole through the semiconductor wafer in an area adjacent to the IC, placing conductive material in the hole, and conductively linking the conductive material to a circuit node on the IC. The preamble of claim 13 is amended to make it clear that the IC is formed <u>within</u> the semiconductor wafer.

HASHIMOTO discloses a method for creating a packaged IC. As illustrated, for example in FIGs 1a, 1b, 14a, 14b, HASHIMOTO teaches mounting an IC chip 1 directly on a PCB or ceramic substrate 6 (see FIG. 1A and column 1, lines 48-50) and then using bond wires 2 to provide signal paths from nodes on the surface of the IC chips to conductors 3 formed on the surface of substrate 6. Conductors 7 and 8 extend the signal paths to a lower side of the PCB substrate 6 which may then be linked to other circuits. HASHIMOTO teaches that conductors 7 may be formed by filling holes in substrate 6 with conductive material (See FIG. 2A) and then cutting substrate 6 along

lines 91 (FIG. 13A/13B) so that conductive material 7 remains on the sides of pieces of the substrate 6 containing IC chips 1 as illustrated in FIGs. 9A and 9B. When the IC chip 1 is then covered with resin 5, the result becomes a type of packaged IC having terminals 8 along its lower surface that may be solder bonded to traces on yet another substrate.

An IC chip, such as HASHIMOTO's IC chip 1 usually begins life as one of a set of IC dice formed within a semiconductor wafer. The dice are then separated to form individual IC chips which may be mounted directly on a conventional printed circuit board (PCB) substrate (or on ceramic or other type of substrate) and then interconnected to other circuit components. The method HASHIMOTO teaches use of bond wires to provide signal paths to nodes on the surfaces of chip 1 provided after chip 1 has been singulated (i.e., after it is cut from the wafer in which it was formed). The applicant's method for fabricating a signal path to nodes on ICs occurs while the ICs are still in wafer form, before the ICs are singulated. The holes are formed in the IC chip itself, not in a substrate upon which the chip is mounted.

The applicant's invention as recited in claim 13 is an improvement over HASHIMOTO's interconnect system because it eliminates the need for installing the IC chip on an intermediary substrate 6 and adding bond wires 2. The applicant's interconnect system also reduces the area on a substrate needed to accommodate the IC chip because connections between the chip and the substrate occur underneath the IC chip and there is no need to provide areas adjacent to the chip to accommodate bond wire terminations. Further, since the signal path provided by the applicants' interconnect system is substantially shorter than the signal path provided by HASHIMOTO's interconnect system and has fewer junctions between dissimilar transmission lines, it is able to provide higher bandwidth signal communication than HASHIMOTO's interconnect system.

Although HASHIMOTO teaches providing signal paths through holes in a PCB or ceramic substrate upon which an IC chip 1 is mounted, HASHIMOTO does not suggest that bond wires 2 could or should be replaced with signal paths created while IC chip 1 was still an un-singulated die by forming a hole in the semiconductor wafer, placing conductive material in the hole and then conductively linking the conducive material residing in the hole to a node on the IC. HASHIMOTO's disclosure has nothing to do with forming holes in

semiconductor wafers for any purpose and nothing in HASHIMOTO would motivate one of skill in the art to do so.

Claim 13 is therefore patentable over HASHIMOTO for the following reasons:

1. HASHIMOTO fails to disclose or suggest the recited step a of forming a hole in a semiconductor wafer adjacent to an area occupied by an IC,

2. HASHIMOTO fails to disclose or suggest the recited step b of placing conductive material in a hole in a semiconductor wafer, and

3. HASHIMOTO fails to disclose or suggest the recited step c of providing a signal path between an IC node and conductive material formed in a hole in a semiconductor wafer within which the IC is formed.

Claim Rejections - 35 USC 103

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 5,832,600 (HASHIMOTO). Claims 14 and 15 depend on claim 13 and are patentable over HASHIMOTO for the similar reasons. Claims 14 and 15 further recite a step of "cutting the wafer along a horizontal saw-line extending across the hole such that the portion of the semiconductor wafer containing the IC includes a peripheral edge formed along the saw-line upon which a portion of the conductive material placed in the hole remains attached.

The Examiner argues that it make no difference whether the HASHIMOTO calls a saw-line a "saw-line", a "dicing line" or a "Michael Jackson-line". The applicant agrees; the difference lies more in what is being sawn, not in what the saw-line is called. HASHIMOTO discloses cutting a PCB or ceramic substrate 6 (as illustrated in FIGs. 13A and 13B) in areas containing holes along a saw-line filled with conductive material, but HASHIMOTO does not disclose or suggest cutting a semiconductor wafer along a saw-line containing a hole filed with conductive material. HASHIMOTO does not discuss semiconductor wafers, and nothing in HASHIMOTO teaches or suggests cutting a semiconductor wafer along saw-lines containing holes filed with conductive material. Nothing in HASHIMOTO suggests that signal paths could or should be formed along edges of the IC die themselves, despite the fact HASHIMOTO could have used the applicant's method for providing signal paths between IC chip 1 and substrate 6 rather than the bond wire method HASHIMOTO teaches, and

despite the fact that the applicant's interconnect method provides very substantial benefits over the bond wire interconnect method. As discussed above, the applicants' interconnect system eliminates the need for bond wires, eliminates the need for an intermediate substrate, reduces chip floor space requirements on the PCB substrate, and provides a substantially higher bandwidth signal path between an IC and a PCB. Claims 14 and 15 are therefore patentable over HASHIMOTO.

Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over HASHIMOTO in view of U.S. patent 6,228,676 (GLENN). Claims 16-18 depend on claim 14 and are patentable over HASHIMOTO for similar reasons. GLENN is similar to HASHIMOTO in that GLENN also discloses a method for creating a packaged IC in which an IC chip 30 is mounted on a substrate 12 having vias 14 passing through the substrate. Bond wires 40 link bond pads on the surface of the chip 30 to vias 14. Thus the subject matter of the parent claim 14 of claims 16-18 is patentable over GLENN for the same reasons discussed distinguishing claim 14 over HASHIMOTO.

Claims 16-18 recite a step of providing second conductive material extending horizontally from the first conductive material along and attached to the lower surface of the semiconductor wafer under the portion of the semiconductor wafer containing the IC. Neither HASHIMOTO nor GLENN disclose conductive material formed on the lower surface of a semiconductor wafer, within which an IC is formed.

The applicant's claims 17 and 18 recite providing second conductive material extending horizontally along and attached to the upper surface of the semiconductor wafer and the IC from the first conductive material to the first circuit node. Neither HASHIMOTO nor GLENN disclose conductive material formed on the upper surface of a semiconductor wafer. Signal paths linked to IC nodes are provided exclusively by bond wires which do not extend horizontally along the upper surface of a semiconductor wafer. GLENN's substrate 12 includes conductive material 22 and 26 on its upper and lower surfaces, but substrate 12 is not a semiconductor wafer. GLENN describes substrate 12 as a "ceramic, a laminate, a passivated metal or a printed circuit board substrate material" (column 2, lines 55-56). Claims 16-18 are therefore patentable over the combination of HASHIMOTO and GLENN.

New claims 33-35 are patentable over HASHIMOTO and GLENN for reasons similar to those discussed in connection with claims 13-18.

The prior art illustrated in the applicant's FIG. 5, includes providing conductive vias in semiconductor wafers, but these vias reside within the same area of the semiconductor wafer in which the IC resides and do not extend vertically through an area of the semiconductor wafer adjacent to the portion of the wafer containing the IC as recited in claim 13. Since the prior art vias reside in the same wafer area as the IC, they consume floor space that could otherwise be occupied by IC devices. By placing the holes outside the IC area as recited in claim 13, the vias do not compete with the IC for floor space.

All prior art references cited by the examiner have been reviewed and do not appear to disclose or suggest the invention as claimed.

It is believed that in view of the foregoing amendments and remarks, the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

Daniel J. Bedell
Reg. No. 30,156

SMITH-HILL & BEDELL, P.C.
12670 NW Barnes Road, Suite 104
Portland, Oregon 97229

Tel. (503) 574-3100
Fax (503) 574-3197
Docket: FORM 2132 (P129)
Postcard: 6/02-52

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on the 17 day of June, 2002.

Penelope Stockwell